What Is Claimed Is:

1. A method of fabricating a pair of single-poly EPROM cells, compatible with CMOS process, comprising:

providing a substrate with an isolation region to define a striped active area;

forming a deep well of first conductive type located under the isolation region and the striped active area;

forming a gate oxide layer on the striped active area;

forming a conductive layer on the substrate having the gate oxide layer formed thereon;

defining the conductive layer to form a pair of floating gates and a pair of selective gates, with a gap between the pair of floating gates and the pair of selective gates, wherein the pair of selective gates are striped and perpendicular to the striped active area, and the pair of selective gates are disposed between the pair of floating gates;

forming a well of second conductive type in the deep well of first conductive type below the pair of selective gates and the pair of floating gates;

forming a pair of sources in the side walls of the well of second conductive type, the pair of sources connected to each other via the deep well of first conductive type; and

forming a drain in the well of second conductive type between the pair of selective gates.

2. The method of claim 1, wherein the isolation region is a field oxide layer.

3. The method of claim 1, wherein the isolation region is a shallow trench isolation.

4. The method of claim 1, wherein the conductive layer is a polysilicon layer.

5. The method of claim 1, wherein the method of forming the pair of floating gates and the pair of selective gates comprises:

forming a mask layer on the conductive layer, the mask layer substantially having the pattern of the pair of floating gates and the pair of selective gates;

forming a plurality of spacers on the side walls of the mask layer, wherein the width of the gap between the pair of floating gates and the pair of selective gates is controlled by the spacers; and

etching the conductive layer using the mask layer's spacers as an etching mask.

6. The method of claim 5, wherein the method of forming the well of second conductive type comprises:

forming a photoresist layer on the substrate on which the mask layer and the spacers are formed, the photoresist layer substantially having a pattern corresponding to the drain and being parallel to pair of selective gates;

implanting dopants of second conductive type in the deep well of first conductive type using the photoresist layer as a mask;

removing the photoresist layer;

thermally driving the dopants so as to form the striped well of second conductive type disposed under the pair of floating gates; and

removing the mask layer and the spacers.

7. The method of claim 1, wherein the step of forming the sources further comprising forming a dielectric layer on the

surface of the conductive layer to fill the gap between the pair of floating gates and the pair of selective gates.

8. A structure of single-poly EPROM which is suitable for using as memory cell in a substrate, comprising:

an isolation region disposed in the substrate to define a striped active area;

a deep well of first conductive type located under the isolation region and the striped active area;

a gate oxide layer disposed on the striped active area on the substrate;

a pair of selective gates disposed on the gate oxide layer and the isolation region, wherein the pair of selective gates are striped and perpendicular to the striped active area;

a pair of floating gates disposed on the gate oxide layer, and are corresponding to the active area, wherein a gap is formed between the pair of floating gates and the pair of selective gates;

a well of second conductive type disposed in the deep well of first conductive type below the pair of selective gates and the pair of floating gates;

a pair of sources disposed on both sides of the well of second conductive type, the pair of sources connected to each other via the deep well of first conductive type; and

a drain disposed in the well of second conductive type between the pair of selective gates.

9. The structure of claim 8, wherein the isolation region is a field oxide layer.

10. The structure of claim 8, wherein the isolation region is a shallow trench isolation.

11. The structure of claim 8, wherein the pair of floating gates and the pair of selective gates are polysilicon.

12. The structure of claim 8, wherein the pair of sources are laterally extended to half the width of the pair of floating gates.

13. A method for programming memory cells of a single-poly EPROM, wherein a pair of memory cells share a drain, the structure thereof comprising:

an isolation region disposed in the substrate to define a striped active area;

a deep well of first conductive type located under the isolation region and the striped active area;

a gate oxide layer disposed on the substrate at the striped active area;

a pair of selective gates disposed on the gate oxide layer and the isolation region, wherein the pair of selective gates are striped and perpendicular to the striped active area;

a pair of floating gates disposed on the gate oxide layer and are corresponding to the active area, wherein a gap is formed between the pair of floating gates and the pair of selective gates;

a well of second conductive type disposed in the deep well of first conductive type below the pair of selective gates and portions of the pair of floating gates;

a pair of sources disposed on both sides of the well of second conductive type, wherein the pair of sources are connected to each other via the deep well of first conductive type; and

a drain disposed in the well of second conductive type between the pair of selective gates;

the method of applying programming bias voltages to a selected memory cell comprising the following steps:

applying a first positive voltage to the selective gate of the selected memory cell, the first positive voltage being about 1.5-2 V;

applying a second positive voltage to the pair of sources, the second positive voltage being about 10-12 V;

grounding the well of second conductive type;

grounding the drain; and

grounding the selective gate of the other unselected memory cell,

wherein the programming bias voltages cause or make charge carriers to perform source side injection (SSI), and accumulate in the floating gate of the selected memory cell.

14. A method for reading memory cell of a single-poly EPROM, wherein a pair of memory cells share a drain, the structure comprising:

an isolation region disposed in the substrate to define a striped active area;

a deep well of first conductive type located under the isolation region and the striped active area;

a gate oxide layer disposed on the striped active area on the substrate;

a pair of selective gates disposed on the gate oxide layer and the isolation region, wherein the pair of selective gates are striped and perpendicular to the striped active area;

a pair of floating gates disposed on the gate oxide layer and are corresponding to the active area, wherein a gap is formed between the pair of floating gates and the pair of selective gates;

a well of second conductive type disposed in the deep well of first conductive type below the pair of selective gates and portions of the pair of floating gates;

a pair of sources disposed on both sides of the well of second conductive type, the pair of sources being connected to each other via the deep well of first conductive type; and

a drain disposed in the well of second conductive type between the pair of selective gates,

the method of applying reading bias voltages to a selected memory cell comprising the following steps:

applying a first positive voltage to the selective gate of the selected memory cell, the first positive voltage being Vcc;

applying a second positive voltage to the drain, the second positive voltage being about 2 V; and

grounding the selective gate of the other unselected memory cell.